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(54) **DISPLAY PANEL OF AN ORGANIC LIGHT EMITTING DIODE DISPLAY DEVICE HAVING A PENTILE PIXEL STRUCTURE**

(71) Applicant: **Samsung Display Co., Ltd**, Yongin-si (KR)

(72) Inventors: **Young-In HWANG**, Suwon-si (KR); **Elly Gil**, Seoul (KR); **Eungtaek Kim**, Hwaseong-si (KR); **Jina Lee**, Seongnam-si (KR); **Joohyeon Jo**, Asan-si (KR); **Seongbaik Chu**, Busan (KR)

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(57) **ABSTRACT**

A display panel of an OLED display device includes a first OLED disposed in a first sub-pixel region, a second OLED disposed in a second sub-pixel region adjacent to the first sub-pixel region in a row direction, a third OLED disposed in a third sub-pixel region adjacent to the first sub-pixel region in a column direction, a fourth OLED disposed in a fourth sub-pixel region adjacent to the second sub-pixel region in the column direction and adjacent to the third sub-pixel region in the row direction, a first sub-pixel circuit disposed in the first sub-pixel region and a fourth sub-pixel circuit disposed in the fourth sub-pixel region, both configured to drive the first OLED, a second sub-pixel circuit disposed in the second sub-pixel region, and configured to drive the fourth OLED, a third sub-pixel circuit disposed in the third sub-pixel region, and configured to drive the third OLED.

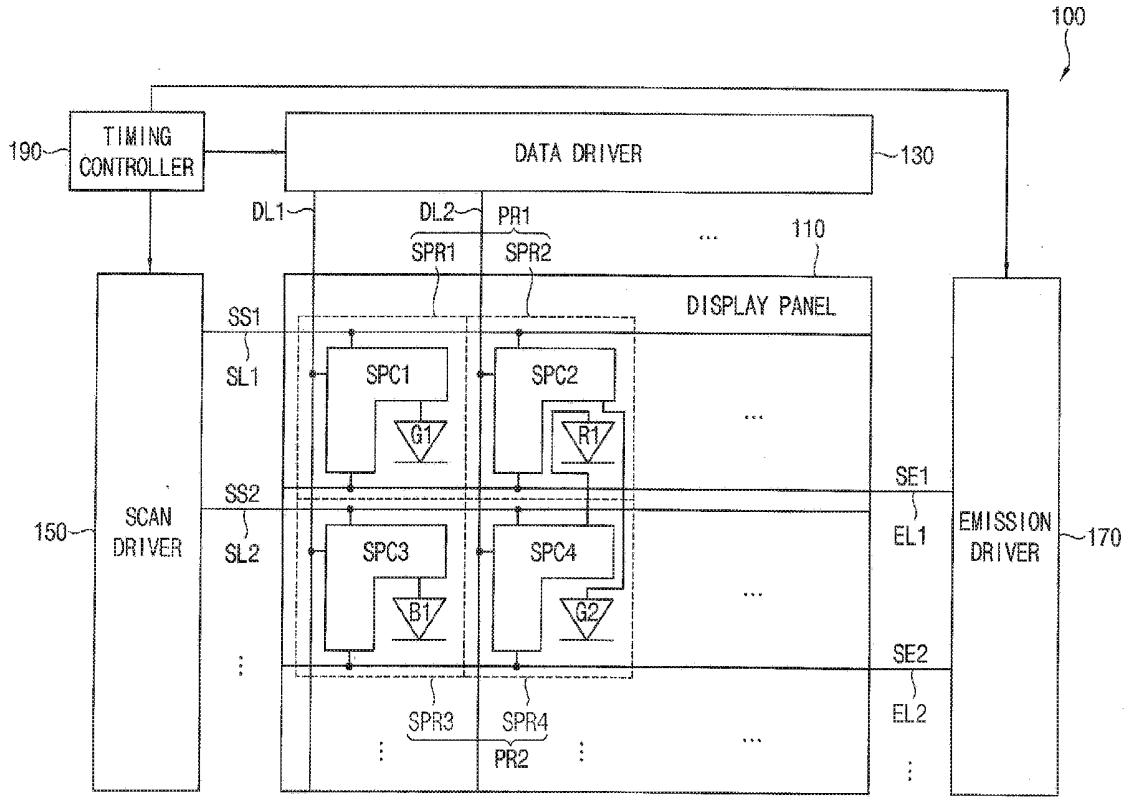
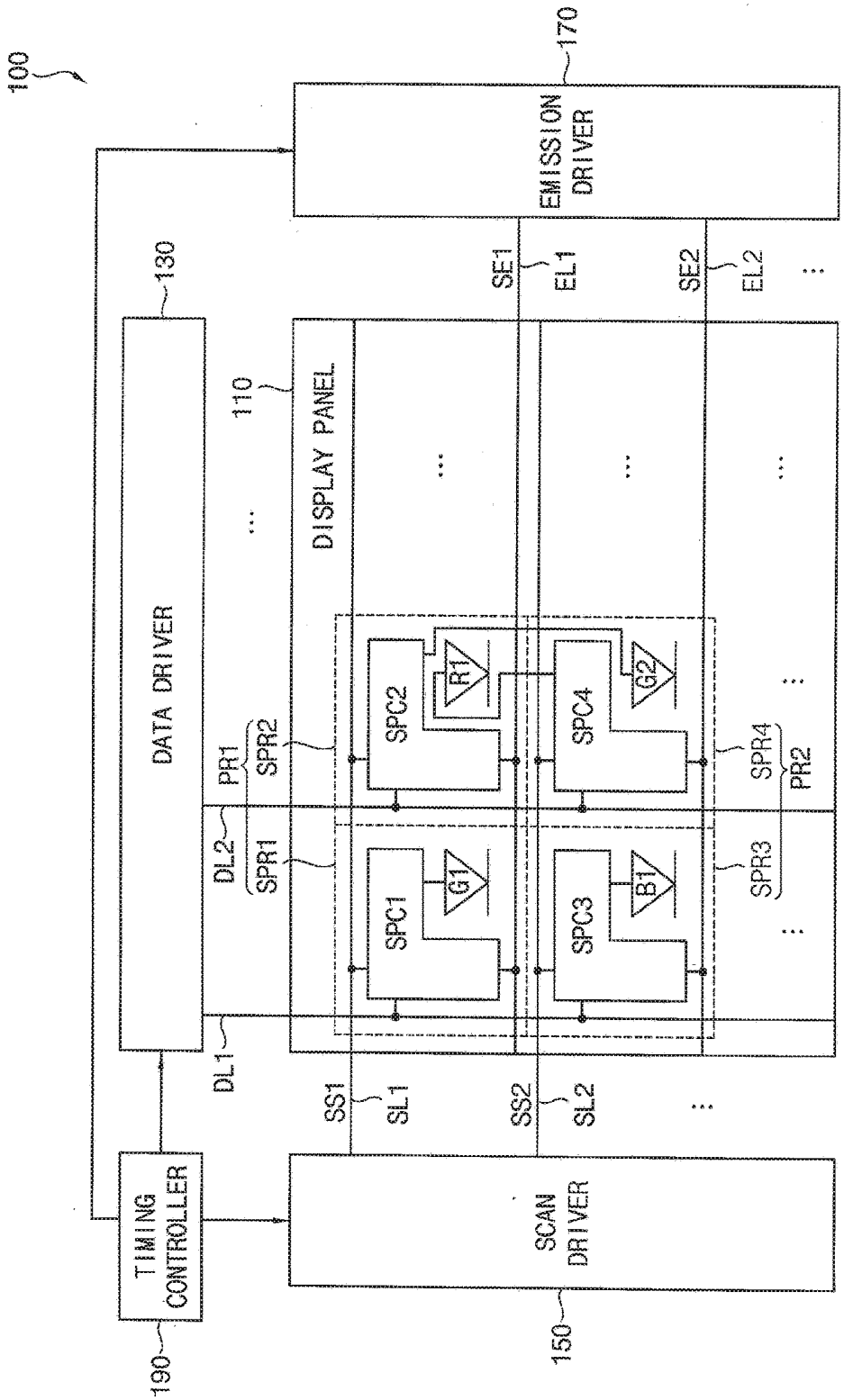


FIG. 1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170
EMISSION DRIVER
130
DATA DRIVER
110
DISPLAY PANEL
SE1
EL1
SE2
EL2
PR1
SPR2
DL2
SPR1
SPC1
G1
SPC2
R1
SPC3
B1
SPC4
G2
SPR4
PR2
SPR3
DL1
SS1
SL1
SS2
SL2
TIMING CONTROLLER
190
SCAN DRIVER
150

FIG. 2

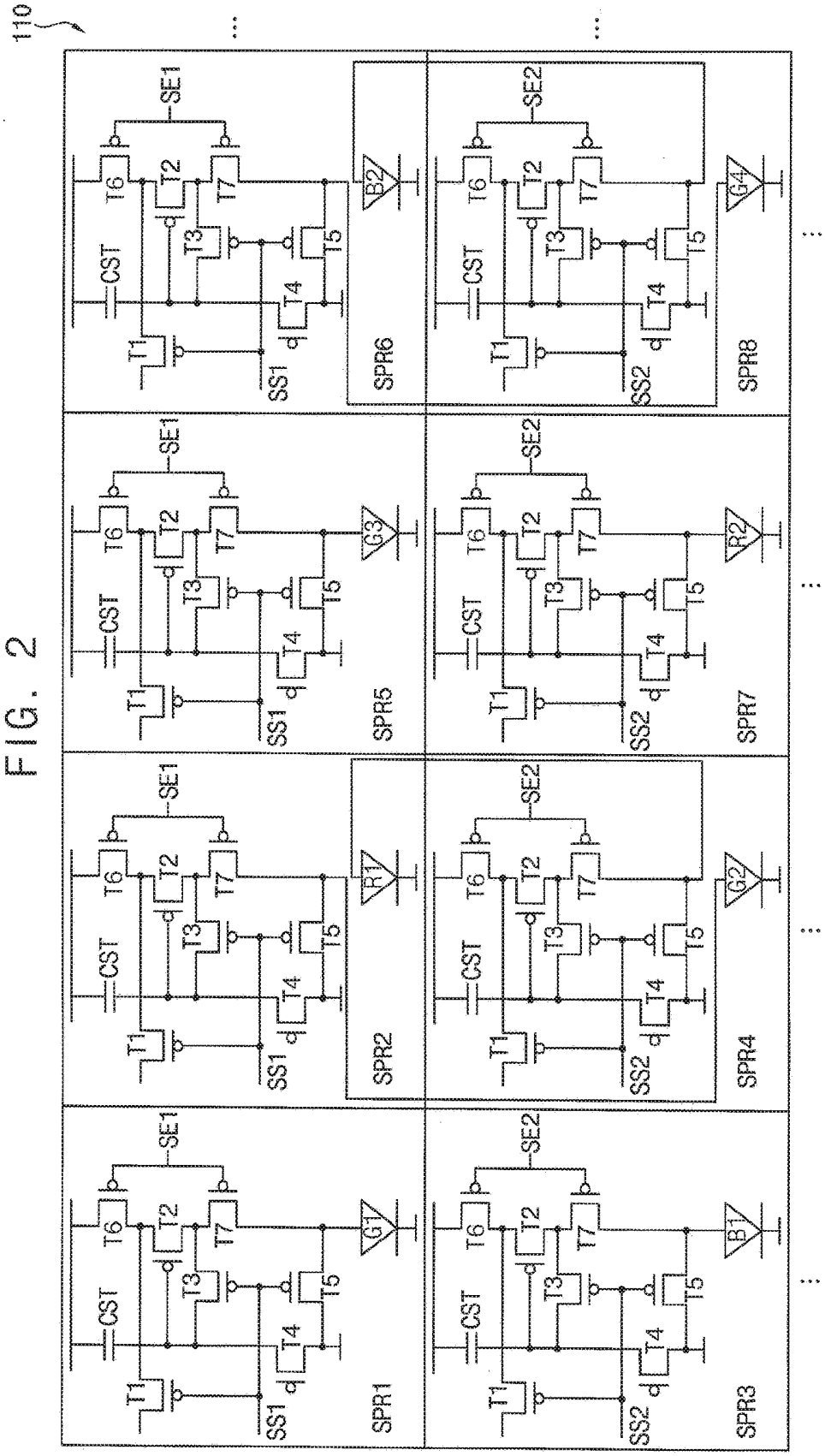

110
SE1
SE2
T1
T2
T3
T4
T5
T6
T7
CST
SS1
SS2
SPR1
SPR2
SPR3
SPR4
SPR5
SPR6
SPR7
SPR8
G1
R1
B1
G2
G3
B2
R2
G4

FIG. 3

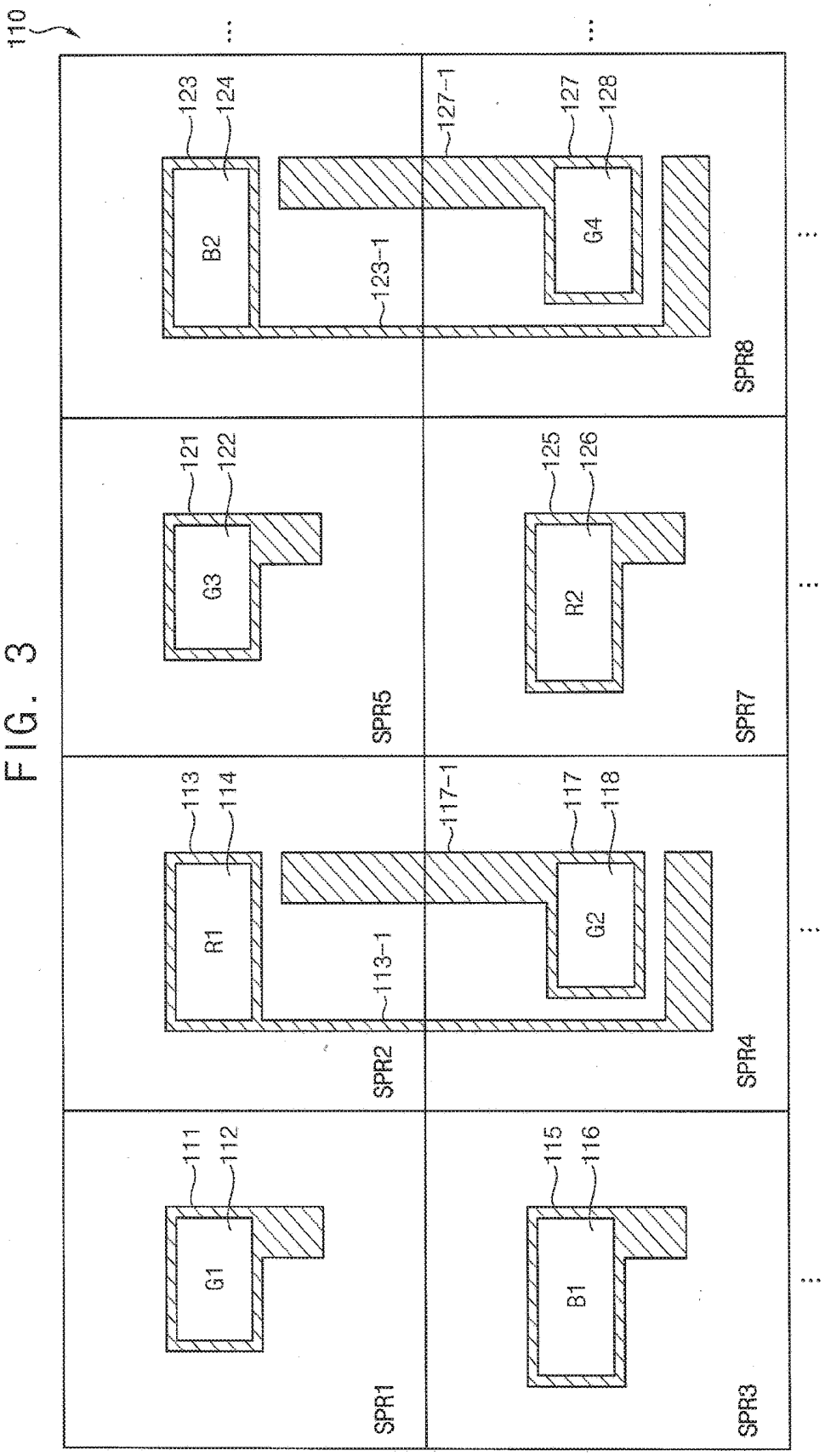

110
123
124
B2
123-1
127-1
127
128
G4
SPR8
121
122
G3
SPR5
125
126
R2
SPR7
113
114
R1
113-1
117-1
117
118
G2
SPR2
SPR4
111
112
G1
SPR1
115
116
B1
SPR3

FIG. 4

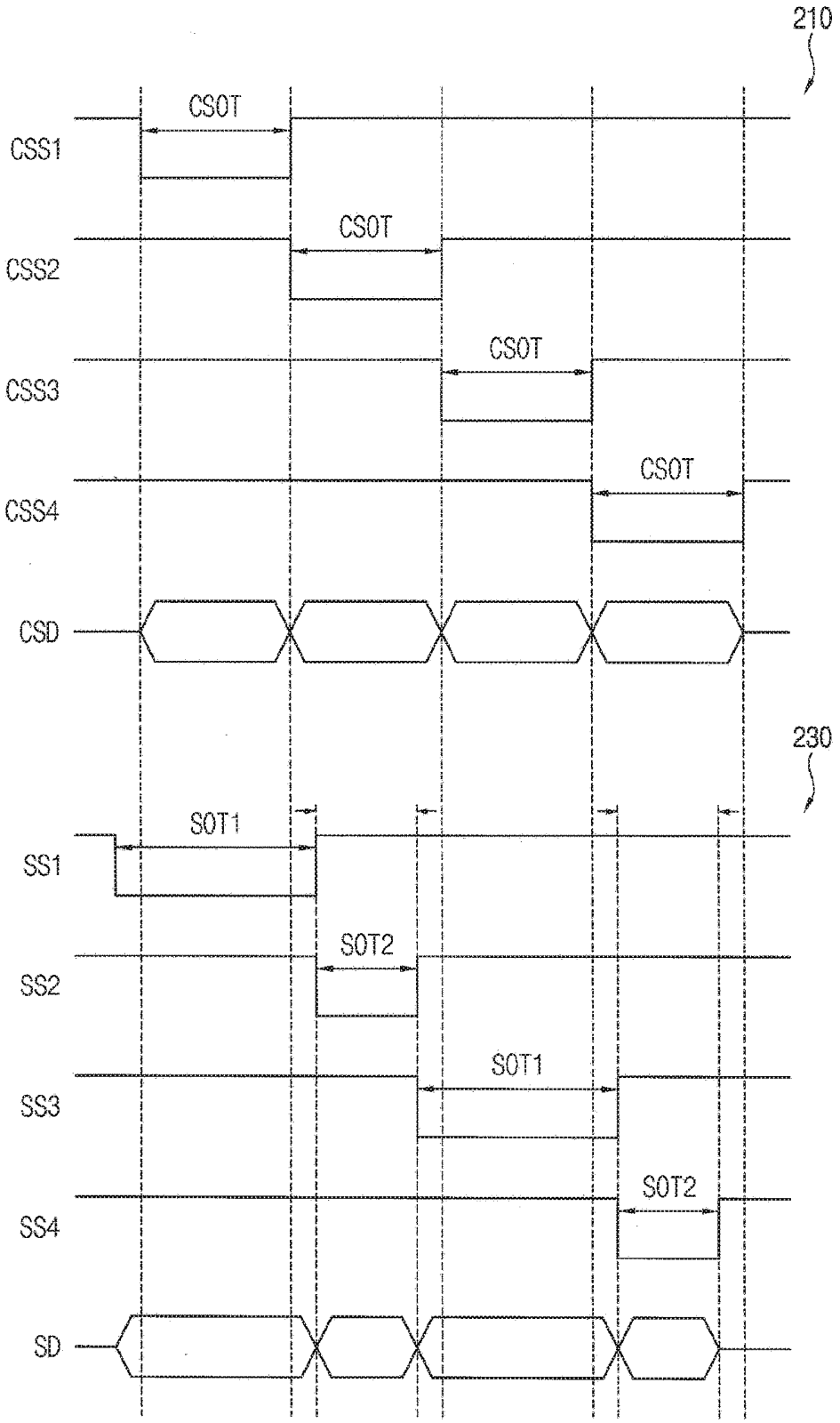

210
CSOT
CSS1
CSOT
CSS2
CSOT
CSS3
CSOT
CSS4
CSD
230
SOT1
SS1
SOT2
SS2
SOT1
SS3
SOT2
SS4
SD

FIG. 5

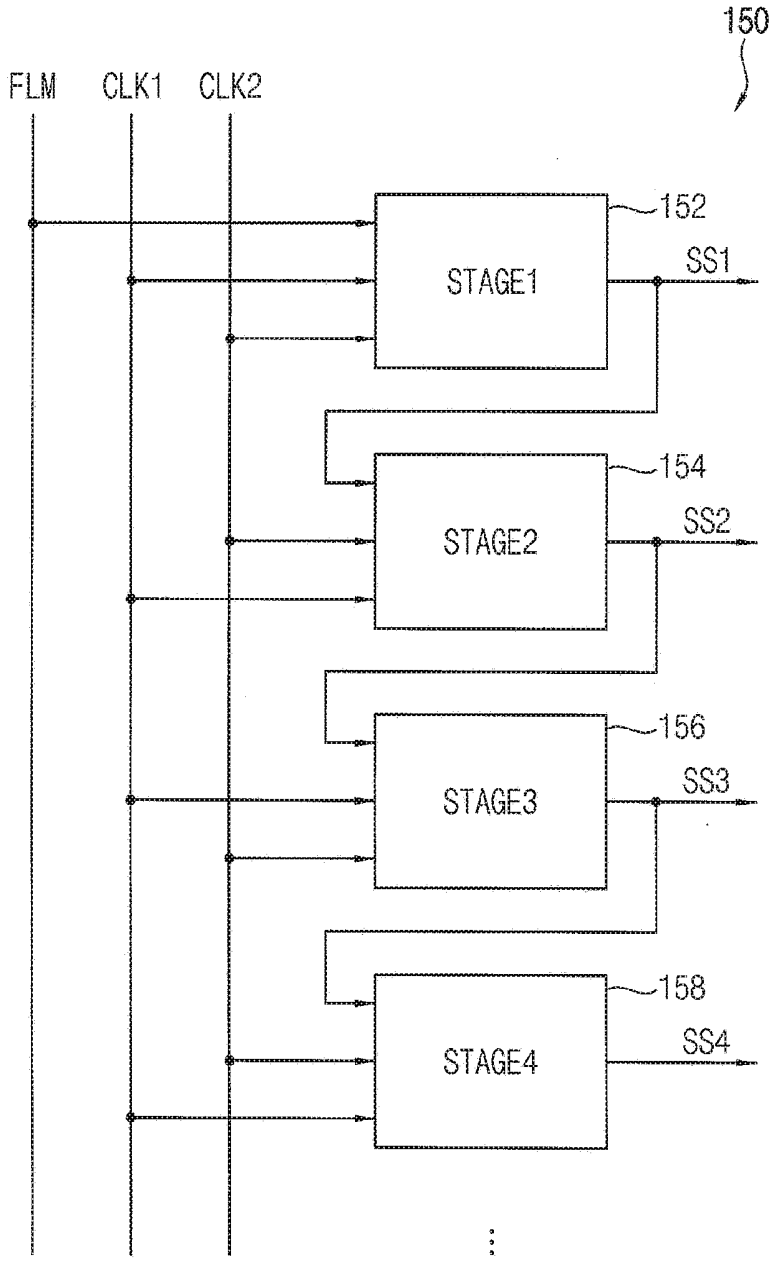

150
FLM
CLK1
CLK2
152
STAGE1
SS1
154
STAGE2
SS2
156
STAGE3
SS3
158
STAGE4
SS4

FIG. 6

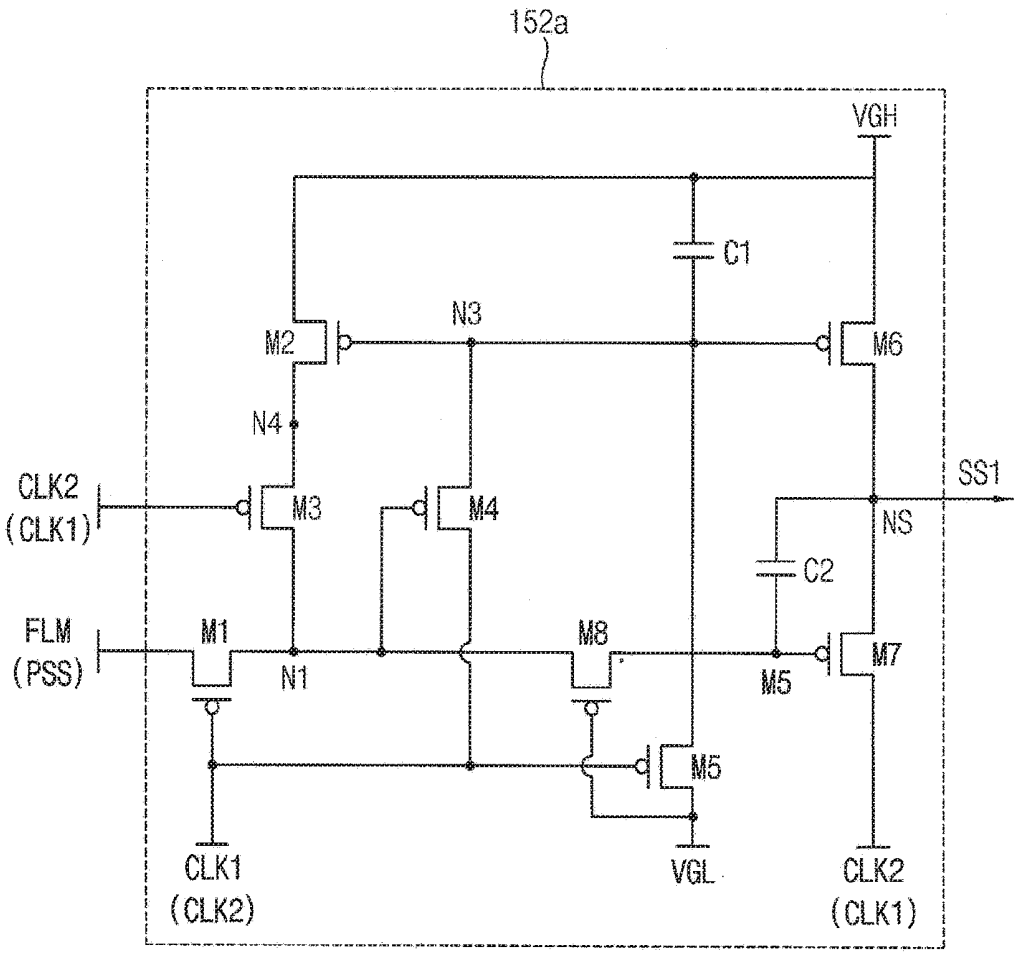

152a
VGH
C1
N3
M2
M6
N4
CLK2
(CLK1)
M3
M4
SS1
NS
C2
FLM
(PSS)
M1
M8
M7
N1
M5
M5
CLK1
(CLK2)
VGL
CLK2
(CLK1)

FIG. 7

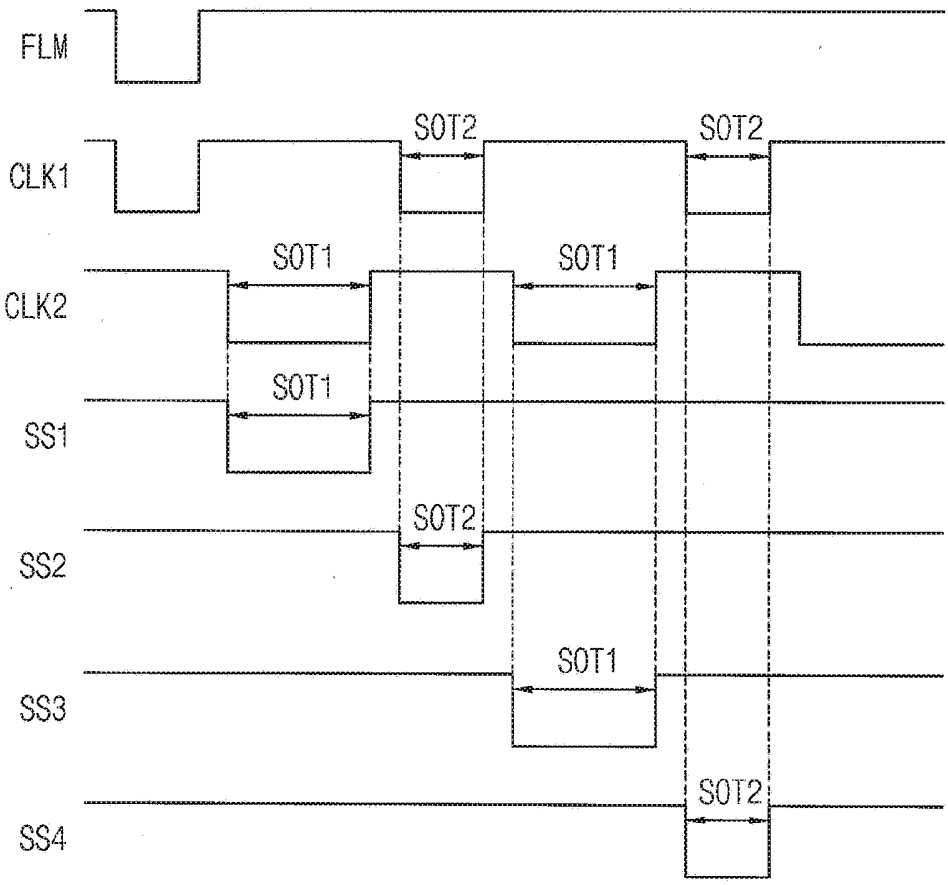


FIG. 8

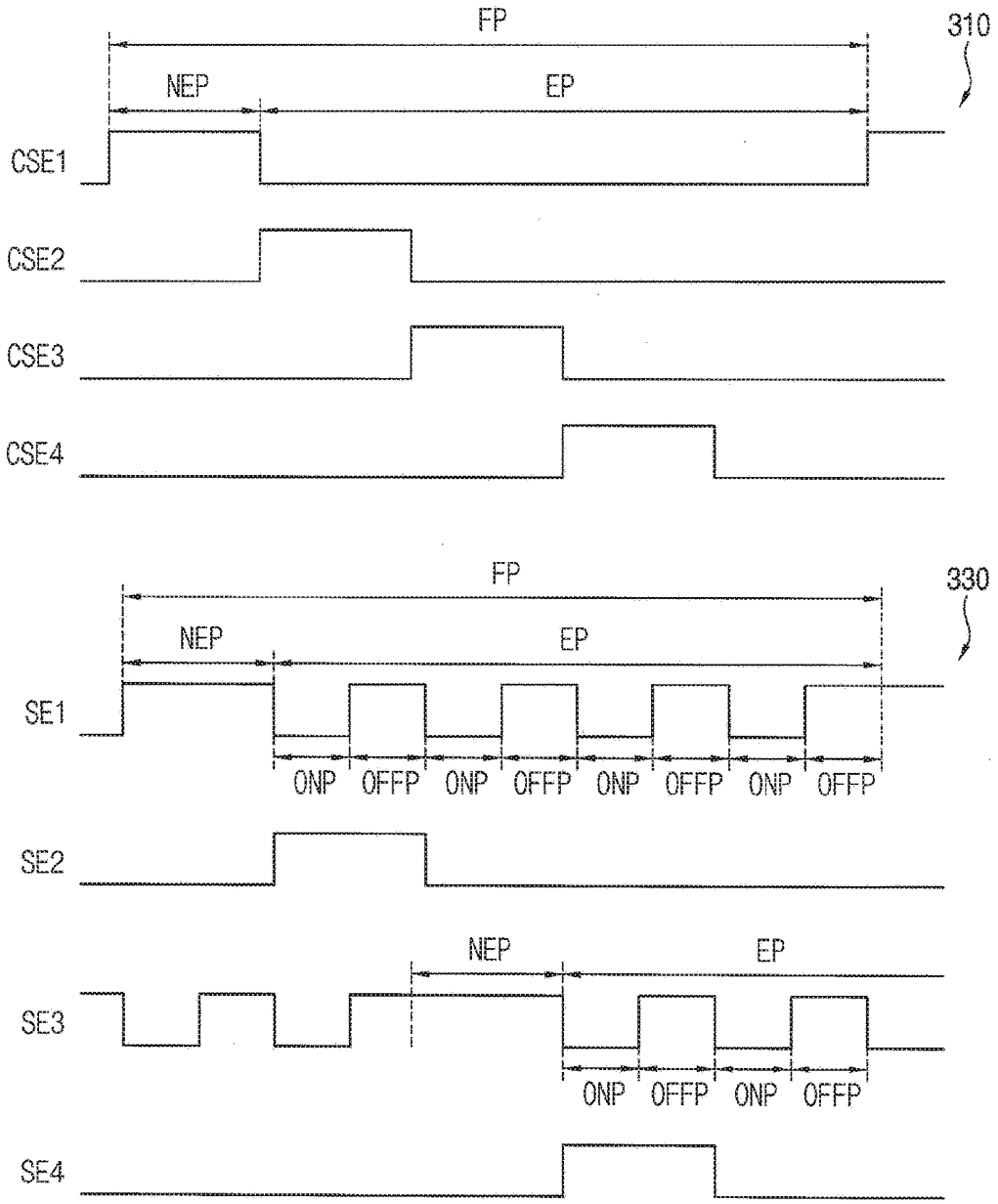

FP
310
NEP
EP
CSE1
CSE2
CSE3
CSE4
FP
330
NEP
EP
SE1
ONP
OFFP
ONP
OFFP
ONP
OFFP
ONP
OFFP
SE2
NEP
EP
SE3
ONP
OFFP
ONP
OFFP
SE4

FIG. 9

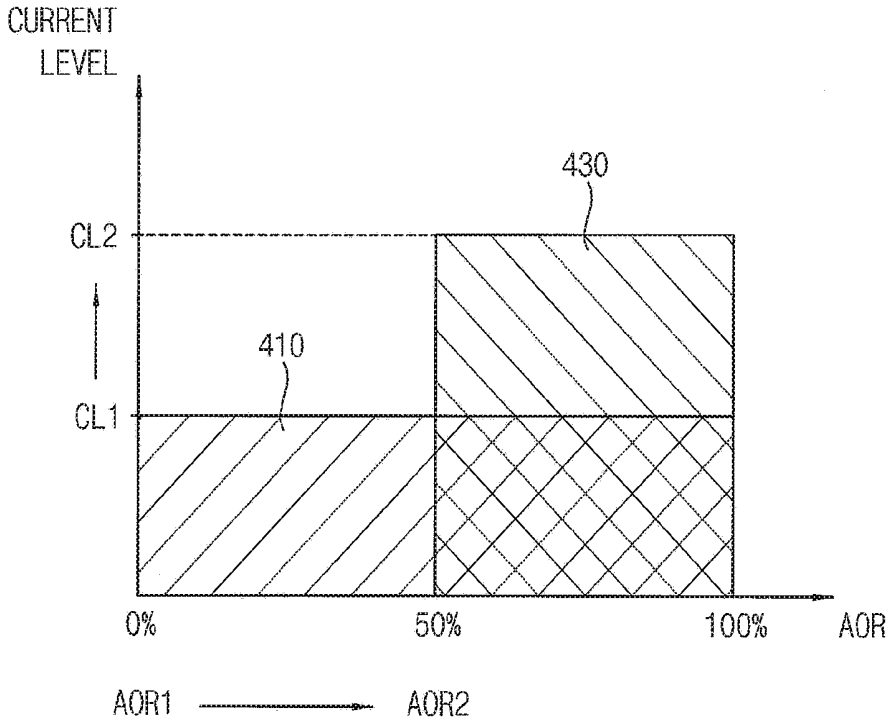
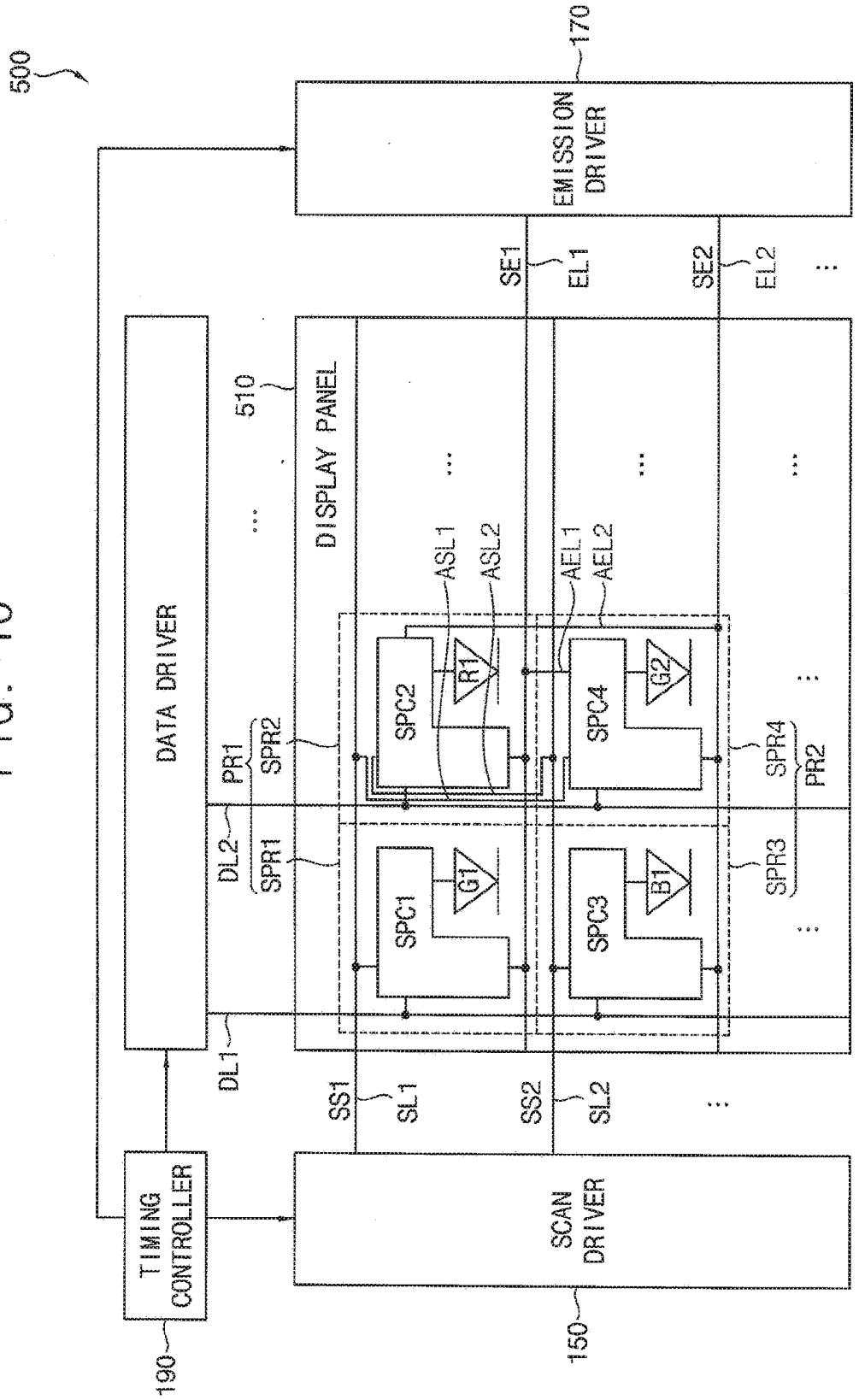


FIG. 10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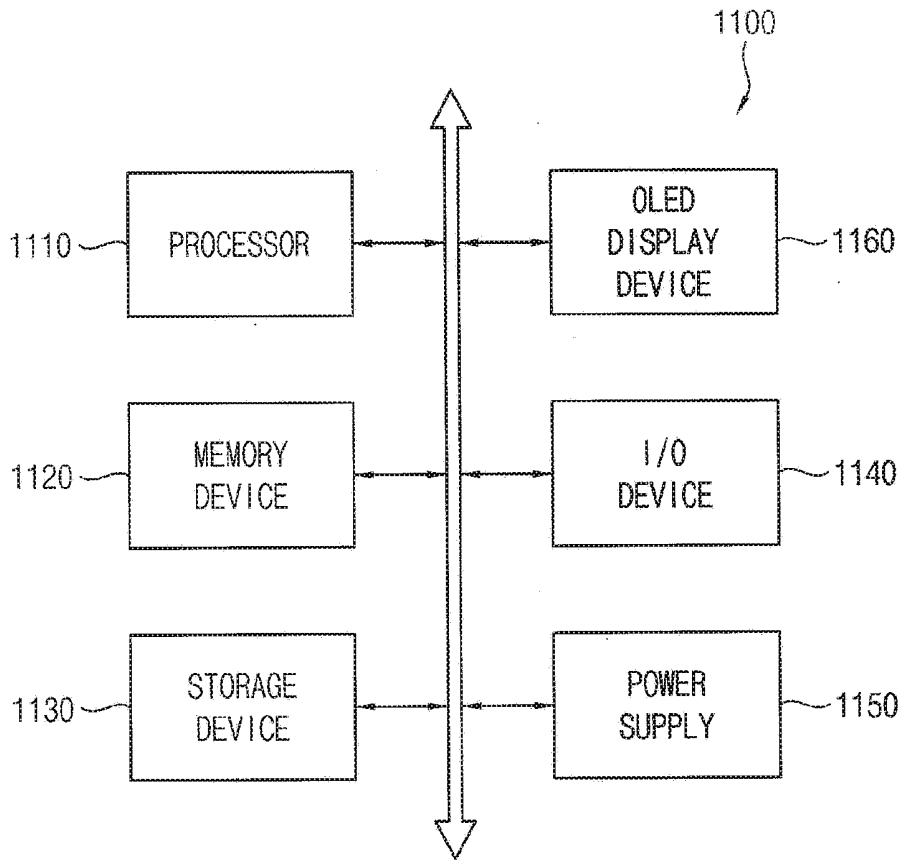
170
EMISSION DRIVER
SE1
EL1
SE2
EL2
DATA DRIVER
510
DISPLAY PANEL
ASL1
ASL2
AEL1
AEL2
SPC2
R1
SPC4
G2
PR1
SPR2
SPR4
PR2
DL2
SPR1
SPR3
SPC1
G1
SPC3
B1
DL1
SS1
SL1
SS2
SL2
TIMING CONTROLLER
SCAN DRIVER
190
150

FIG. 11


1100
1110
PROCESSOR
OLED DISPLAY DEVICE
1160
1120
MEMORY DEVICE
I/O DEVICE
1140
1130
STORAGE DEVICE
POWER SUPPLY
1150

DISPLAY PANEL OF AN ORGANIC LIGHT EMITTING DIODE DISPLAY DEVICE HAVING A PENTILE PIXEL STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority from and the benefit of Korean Patent Applications No. 10-2018-0026529, filed on Mar. 6, 2018, which is hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND

Field

[0002] Exemplary implementations of the invention relate generally to display devices and, more particularly, to display panels of organic light emitting diode (OLED) display devices having pentile pixel structures.

Discussion of the Background

[0003] To display a full color image, each pixel of an organic light emitting diode (OLED) display device may include sub-pixels emitting light of different colors, for example, red, green and blue sub-pixels. In a conventional OLED display device, the red, green and blue sub-pixels may be arranged in a linear form such that sub-pixels of the same color are arranged in each column.

[0004] Recently, to increase a resolution of a display screen, an OLED display device having a pentile pixel structure where a blue sub-pixel and/or a red sub-pixel are shared by two adjacent pixels has been developed. As used herein "pentile" refers to pixel structure in an OLED display device in which each pixel has two sub-pixels including one green sub-pixel and one red or blue sub-pixel, such as the RGBG matrix sub-pixel design marketed by the assignee of this application under its PenTile® trademark. Accordingly, in a pentile pixel structure, the pixel size may be reduced, and thus resolution of the OLED display device may be increased.

[0005] However, in a conventional OLED display device having the pentile pixel structure, all of the red, green and blue sub-pixels are disposed in the same row, and thus the red, green and blue sub-pixels are driven under the same driving condition (e.g., the same scan on time, the same emission time, etc.).

[0006] The above information disclosed in this Background section is only for understanding of the background of the inventive concepts, and, therefore, it may contain information that does not constitute prior art.

SUMMARY

[0007] Applicant discovered that driving the pixels in an OLED having a pentile pixel structure in the conventional line by line manner can cause defects in the display during operation including the appearance of a mura and/or an afterimage.

[0008] In a display panel of an organic light emitting diode (OLED) display device having a pentile pixel structure constructed according to the principles and exemplary implementations of the invention, an OLED of a first color (e.g., a green color) can be driven under a driving condition (e.g., a scan on time, an emission time, different off period ratios, etc.) different from a driving condition for an OLED of another color, thereby reducing occurrence of display defects such as muras and afterimages.

[0009] For example, as described herein, OLEDs in a display device may be alternately arranged in a pentile structure such that each pixel region includes an OLED of a first color (e.g., a green color) and one of an OLED of a second color (e.g., a red color) or an OLED of a third color (e.g., a blue color). Further, in one column (e.g., an even-numbered column) per two columns, an OLED in an odd-numbered row may be driven by a sub-pixel circuit in an even-numbered row, and an OLED in the even-numbered row may be driven by a sub-pixel circuit in the odd-numbered row. Accordingly, the OLED of the first color (e.g., the green color) can be driven under a driving condition (e.g., a scan on time, an AMOLED off ratio (AOR), etc.) that is different from the driving condition for the OLEDs of the second and third colors, and thus a mura and/or an afterimage may be reduced.

[0010] According to another advantageous feature that may be implemented in some embodiments of the invention, the first threshold voltage compensation time for the driving transistor included in the sub-pixel circuit driving two OLED's of one color (such as green) may be longer than the second threshold voltage compensation time for the driving transistor included in the sub-pixel circuit driving the other color OLED (such as red or green). Thus the sub-pixel circuit(s) driving the one color OLED (such as green) that is vulnerable to a mura may perform a threshold voltage compensation operation for a sufficient threshold voltage compensation time to is reduce or prevent mura in the display. According to yet another advantageous feature that may be implemented in some embodiments of the invention, the sub-pixel circuits receiving a first emission control signal may provide the two OLEDs light of the first color (e.g., green) with a driving current that is increased compared to first off period ratio. Accordingly, the OLED display device according to some exemplary embodiments may allow the driving transistors of the sub-pixel circuits to generate increased or higher driving current, thereby reducing an afterimage caused by a hysteresis of the driving transistors.

[0011] Additional features of the inventive concepts will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the inventive concepts.

[0012] According to one or more exemplary embodiments, a display panel of an OLED display device, the display panel includes a first OLED disposed in a first sub-pixel region, and configured to emit light of a first color, a second OLED disposed in a second sub-pixel region adjacent to the first sub-pixel region in a row direction, and configured to emit light of a second color, a third OLED disposed in a third sub-pixel region adjacent to the first sub-pixel region in a column direction, and configured to emit light of a third color, a fourth OLED disposed in a fourth sub-pixel region adjacent to the second sub-pixel region in the column direction and adjacent to the third sub-pixel region in the row direction, and configured to emit light of the first color, a first sub-pixel circuit disposed in the first sub-pixel region, and configured to drive the first OLED in the first sub-pixel region, a second sub-pixel circuit disposed in the second sub-pixel region, and configured to drive the fourth OLED in the fourth sub-pixel region, a third sub-pixel circuit disposed in the third sub-pixel region, and configured to drive the third OLED in the third sub-pixel

region, and a fourth sub-pixel circuit disposed in the fourth sub-pixel region, and configured to drive the second OLED in the second sub-pixel region.

[0013] The first and fourth OLEDs may be green OLEDs configured to emit green light, the second OLED may be a red OLED configured to emit red light, and the third OLED may be a blue OLED configured to emit blue light.

[0014] The second OLED in the second sub-pixel region may include an anode extension portion connected to the fourth sub-pixel circuit, and the fourth OLED in the fourth sub-pixel region may include another anode extension portion connected to the second sub-pixel circuit in the second sub-pixel region.

[0015] The first and second sub-pixel circuits may each receives a first scan signal having substantially the same value through a first scan line, and the third and fourth sub-pixel circuits may each receives a second scan signal having substantially the same value through a second scan line.

[0016] A first scan on time (SOT) of the first scan signal applied to the first and second sub-pixel circuits may be different from a second SOT of the second scan signal applied to the third and fourth sub-pixel circuits.

[0017] A first SOT of the first scan signal applied to the first and second sub-pixel circuits may be longer than a second SOT of the second scan signal applied to the third and fourth sub-pixel circuits.

[0018] The first and second sub-pixel circuits may further include first driving transistors, the third and fourth sub-pixel circuits may further include second driving transistors, a first threshold voltage compensation time for the first driving transistors included in the first and second sub-pixel circuits may be longer than a second threshold voltage compensation time for the second driving transistors included in the third and fourth sub-pixel circuits.

[0019] The first and second sub-pixel circuits may receive a first emission control signal having substantially the same value through a first emission control line, and the third and fourth sub-pixel circuits may receive a second emission control signal having substantially the same value through a second emission control line.

[0020] A first off period ratio of the first emission control signal applied to the first and second sub-pixel circuits may be different from a second off period ratio of the second emission control applied to the third and fourth sub-pixel circuits.

[0021] A first off period ratio of the first emission control signal applied to the first and second sub-pixel circuits may be greater than a second off period ratio of the second emission control applied to the third and fourth sub-pixel circuits.

[0022] The first and second sub-pixel circuits may drive the first and fourth OLEDs to emit the light of the first color with the first off period ratio that is increased from the second off period ratio for the second and third OLEDs.

[0023] The first and second sub-pixel circuits may provide the first and fourth OLEDs with a driving current corresponding to the increased first off period ratio, the driving current may be provided to the first and fourth OLEDs and might be greater than driving current provided to the second and third OLEDs.

[0024] According to one or more exemplary embodiments, a display panel of an OLED display device includes a first OLED disposed in a first sub-pixel region, and configured to emit light of a first color, a second OLED disposed in a second sub-pixel region adjacent to the first sub-pixel region in a row direction, and configured to emit light of a second color, a third OLED disposed in a third sub-pixel region adjacent to the first sub-pixel region in a column direction, and configured to emit light of a third color, a fourth OLED disposed in a fourth sub-pixel region adjacent to the second sub-pixel region in the column direction and adjacent to the third sub-pixel region in the row direction, and configured to emit light of the first color, a first sub-pixel circuit configured to drive the first OLED, a second sub-pixel circuit configured to drive the second OLED, a third sub-pixel circuit configured to drive the third OLED, a fourth sub-pixel circuit configured to drive the fourth OLED, a first scan line extending in the row direction through the first sub-pixel region and the second sub-pixel region, and connected to the first sub-pixel circuit, a second scan line extending in the row direction through the third sub-pixel region and the fourth sub-pixel region, and connected to the third sub-pixel circuit, a first auxiliary scan line connecting the first scan line to the fourth sub-pixel circuit, and a second auxiliary scan line connecting the second scan line to the third sub-pixel circuit.

[0025] The first sub-pixel may receive a first scan signal through the first scan line, the fourth sub-pixel circuit is configured to may be configured to receive the first scan signal through the first scan line and the first auxiliary scan line, the third sub-pixel circuit may be configured to receive a second scan signal through the second scan line, and the second sub-pixel circuit may be configured to receive the second scan signal through the second scan line and the second auxiliary scan line.

[0026] A first scan on time (SOT) of the first scan signal applied to the first and fourth sub-pixel circuits may be longer than a second SOT of the second scan signal applied to the second and third sub-pixel circuits.

[0027] The display panel may further include a first emission control line extending in the row direction through the first sub-pixel region and the second sub-pixel region, and connected to the first sub-pixel circuit, a second emission control line extending in the row direction through the third sub-pixel region and the fourth sub-pixel region, and connected to the third sub-pixel circuit, a first auxiliary emission control line connecting the first emission control line to the fourth sub-pixel circuit, and a second auxiliary emission control line connecting the second emission control line to the third sub-pixel circuit.

[0028] The first sub-pixel circuit may be configured to receive a first emission control signal through the first emission control line, the fourth sub-pixel circuit may be configured to receive the first emission control signal through the first emission control line and the first auxiliary emission control line, the third sub-pixel circuit may be configured to receive a second emission control signal through the second emission control line, and the second sub-pixel circuit may be configured to receive the second emission control signal through the second emission control line and the second auxiliary emission control line.

[0029] A first off period ratio of the first emission control signal applied to the first and fourth sub-pixel circuits may be greater than a second off period ratio of the second emission control applied to the second and third sub-pixel circuits.

[0030] The first and fourth sub-pixel circuits may be configured to drive the first and fourth OLEDs to emit the light of the first color with the first off period ratio that is increased compared to the second off period ratio for the second and third OLEDs.

[0031] According to one or more exemplary embodiments, an OLED display device includes a display panel, a data driver configured to provide data signals to the display panel, a scan driver configured to provide scan signals to the display panel, an emission driver configured to provide emission control signals to the display panel, and a timing controller configured to control the data driver, the scan driver and the emission driver. The display panel includes a first OLED disposed in a first sub-pixel region, and configured to emit light of a first color, a second OLED disposed in a second sub-pixel region adjacent to the first sub-pixel region in a row direction, and configured to emit light of a second color, a third OLED disposed in a third sub-pixel region adjacent to the first sub-pixel region in a column direction, and configured to emit light of a third color, a fourth OLED disposed in a fourth sub-pixel region adjacent to the second sub-pixel region in the column direction and adjacent to the third sub-pixel region in the row direction, and configured to emit light of the first color, a first sub-pixel circuit disposed in the first sub-pixel region, and configured to drive the first OLED in the first sub-pixel region, a second sub-pixel circuit disposed in the second sub-pixel region, and configured to drive the fourth OLED in the fourth sub-pixel region, a third sub-pixel circuit disposed in the third sub-pixel region, and configured to drive the third OLED in the third sub-pixel region, and a fourth sub-pixel circuit disposed in the fourth sub-pixel region, and configured to drive the second OLED in the second sub-pixel region.

[0032] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0033] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate exemplary embodiments of the invention, and together with the description serve to explain the inventive concepts.

[0034] FIG. **1** is a block diagram illustrating an organic light emitting diode (OLED) display device constructed according to the principles and an exemplary embodiment of the invention.

[0035] FIG. **2** is a circuit diagram illustrating the display panel of FIG. **1**.

[0036] FIG. **3** is a diagram illustrating an exemplary layout of OLEDs included in the display panel of FIG. **1**.

[0037] FIG. **4** is a timing diagram illustrating scan signals of a conventional OLED display device and scan signals of an OLED display device constructed according to the principles and exemplary embodiments of the invention.

[0038] FIG. **5** is a block diagram illustrating a scan driver included in an OLED display device constructed according to an exemplary embodiment of the invention.

[0039] FIG. **6** is a circuit diagram illustrating an example of each stage included in the scan driver of FIG. **5**.

[0040] FIG. **7** is a timing diagram for describing an example of an operation of the scan driver of FIG. **5**.

[0041] FIG. **8** is a timing diagram illustrating emission control signals of a conventional OLED display device and emission control signals of an OLED display device constructed according to the principles and exemplary embodiments of the invention.

[0042] FIG. **9** is a graph illustrating the increase of a driving current level according to the increase of an AMOLED off ratio (AOR) in an OLED display device constructed according to the principles and exemplary embodiments of the invention.

[0043] FIG. **10** is a block diagram illustrating an OLED display device constructed according to the principles and another exemplary embodiment of the invention.

[0044] FIG. **11** is a block diagram illustrating an electronic device including an OLED display device constructed according to the principles and an exemplary embodiment of the invention.

DETAILED DESCRIPTION

[0045] In the following description, for the purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of various exemplary embodiments or implementations of the invention. As used herein "embodiments" and "implementations" are interchangeable words that are non-limiting examples of devices or methods employing one or more of the inventive concepts disclosed herein. It is apparent, however, that various exemplary embodiments may be practiced without these specific details or with one or more equivalent arrangements. In other instances, well-known structures and devices are shown in block diagram form in order to avoid unnecessarily obscuring various exemplary embodiments. Further, various exemplary embodiments may be different, but do not have to be exclusive. For example, specific shapes, configurations, and characteristics of an exemplary embodiment may be used or implemented in another exemplary embodiment without departing from the inventive concepts.

[0046] Unless otherwise specified, the illustrated exemplary embodiments are to be understood as providing exemplary features of varying detail of some ways in which the inventive concepts may be implemented in practice. Therefore, unless otherwise specified, the features, components, modules, layers, films, panels, regions, and/or aspects, etc. (hereinafter individually or collectively referred to as "elements"), of the various embodiments may be otherwise combined, separated, interchanged, and/or rearranged without departing from the inventive concepts.

[0047] The use of cross-hatching and/or shading in the accompanying drawings is generally provided to clarify boundaries between adjacent elements. As such, neither the presence nor the absence of cross-hatching or shading conveys or indicates any preference or requirement for particular materials, material properties, dimensions, proportions, commonalities between illustrated elements, and/or any other characteristic, attribute, property, etc., of the elements, unless specified. Further, in the accompanying drawings, the size and relative sizes of elements may be exaggerated for clarity and/or descriptive purposes. When an exemplary embodiment may be implemented differently, a specific process order may be performed differently from the described order. For example, two consecutively described processes may be performed substantially at the

same time or performed in an order opposite to the described order. Also, like reference numerals denote like elements.

[0048] When an element, such as a layer, is referred to as being "on," "connected to," or "coupled to" another element or layer, it may be directly on, connected to, or coupled to the other element or layer or intervening elements or layers may be present. When, however, an element or layer is referred to as being "directly on," "directly connected to," or "directly coupled to" another element or layer, there are no intervening elements or layers present. To this end, the term "connected" may refer to physical, electrical, and/or fluid connection, with or without intervening elements. Further, the D1-axis, the D2-axis, and the D3-axis are not limited to three axes of a rectangular coordinate system, such as the x, y, and z-axes, and may be interpreted in a broader sense. For example, the D1-axis, the D2-axis, and the D3-axis may be perpendicular to one another, or may represent different directions that are not perpendicular to one another. For the purposes of this disclosure, "at least one of X, Y, and Z" and "at least one selected from the group consisting of X, Y, and Z" may be construed as X only, Y only, Z only, or any combination of two or more of X, Y, and Z, such as, for instance, XYZ, XYY, YZ, and ZZ. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0049] Although the terms "first," "second," etc. may be used herein to describe various types of elements, these elements should not be limited by these terms. These terms are used to distinguish one element from another element. Thus, a first element discussed below could be termed a second element without departing from the teachings of the disclosure.

[0050] Spatially relative terms, such as "beneath," "below," "under," "lower," "above," "upper," "over," "higher," "side" (e.g., as in "sidewall"), and the like, may be used herein for descriptive purposes, and, thereby, to describe one elements relationship to another element(s) as illustrated in the drawings. Spatially relative terms are intended to encompass different orientations of an apparatus in use, operation, and/or manufacture in addition to the orientation depicted in the drawings. For example, if the apparatus in the drawings is turned over, elements described as "below" or "beneath" other elements or features would then be oriented "above" the other elements or features. Thus, the exemplary term "below" can encompass both an orientation of above and below. Furthermore, the apparatus may be otherwise oriented (e.g., rotated 90 degrees or at other orientations), and, as such, the spatially relative descriptors used herein interpreted accordingly.

[0051] The terminology used herein is for the purpose of describing particular embodiments and is not intended to be limiting. As used herein, the singular forms, "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. Moreover, the terms "comprises," "comprising," "includes," and/or "including," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, components, and/or groups thereof, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof. It is also noted that, as used herein, the terms "substantially," "about," and other similar terms, are used as terms of approximation and not as terms of degree, and, as such, are utilized to account for inherent deviations in measured, calculated, and/or provided values that would be recognized by one of ordinary skill in the art.

[0052] As customary in the field, some exemplary embodiments are described and illustrated in the accompanying drawings in terms of functional blocks, units, and/or modules. Those skilled in the art will appreciate that these blocks, units, and/or modules are physically implemented by electronic (or optical) circuits, such as logic circuits, discrete components, microprocessors, hard-wired circuits, memory elements, wiring connections, and the like, which may be formed using semiconductor-based fabrication techniques or other manufacturing technologies. In the case of the blocks, units, and/or modules being implemented by microprocessors or other similar hardware, they may be programmed and controlled using software (e.g., microcode) to perform various functions discussed herein and may optionally be driven by firmware and/or software. It is also contemplated that each block, unit, and/or module may be implemented by dedicated hardware, or as a combination of dedicated hardware to perform some functions and a processor (e.g., one or more programmed microprocessors and associated circuitry) to perform other functions. Also, each block, unit, and/or module of some exemplary embodiments may be physically separated into two or more interacting and discrete blocks, units, and/or modules without departing from the scope of the inventive concepts. Further, the blocks, units, and/or modules of some exemplary embodiments may be physically combined into more complex blocks, units, and/or modules without departing from the scope of the inventive concepts.

[0053] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure is a part. Terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and should not be interpreted in an idealized or overly formal sense, unless expressly so defined herein.

[0054] FIG. **1** is a block diagram illustrating an organic light emitting diode (OLED) display device constructed according to the principles and an exemplary embodiment of the invention.

[0055] Referring to FIG. **1**, an organic light emitting diode (OLED) display device may include a display panel **110**, a data driver **130** which provides data signals to the display panel **110**, a scan driver **150** which provides scan signals SS**1** and SS**2** to the display panel **110**, an emission driver **170** which provides emission control signals SE**1** and SE**2** to the display panel **110**, and a timing controller **190** which controls the data driver **130**, the scan driver **150** and the emission driver **170**.

[0056] The display panel **110** may have a plurality of pixel regions PR**1** and PR**2**, and each pixel region PR**1** and PR**2** may include two sub-pixel regions SPR**1** and SPR**2**, and SPR**3** and SPR**4**, respectively. Further, in each sub-pixel region SPR**1**, SPR**2**, SPR**3** and SPR**4**, one OLED of G**1**, R**1**, B**1** and G**2** and one sub-pixel circuit of SPC**1**, SPC**2**, SPC**3** and SPC**4** may be disposed.

[0057] In the display panel **110**, the OLEDs G**1**, R**1**, B**1** and G**2** may be arranged in a pentile structure such that, in each pixel region PR**1** and PR**2**, one OLED G**1** and G**2** of a first color (e.g., a green color) is disposed, and one OLED R**1** of a second color (e.g., a red color) or one OLED B**1** of

a third color (e.g., a blue color) is alternately disposed. For example, as illustrated in FIG. **1**, a first OLED G**1** emitting the green light and a second OLED R**1** emitting the red light may be disposed in a first pixel region PR**1**, and a third OLED B**1** emitting the blue light and a fourth OLED G**2** emitting the green light may be disposed in a second pixel region PR**2** adjacent to the first pixel region PR**1** in a column direction (e.g., a direction of a data line DL**1** and DL**2**). Thus, since two sub-pixels including one green OLED G**1** and G**2** and one red or blue OLED R**1** and B**1** are disposed in each pixel region PR**1** and PR**2**, the display panel **110** may have a high resolution compared with a conventional display panel where each pixel includes three or more sub-pixels (e.g., red, green and blue sub-pixels). In some exemplary embodiments, as illustrated in FIGS. **1**, **2**, and **3**, green, red, green and blue OLEDs may be sequentially and repeatedly arranged (i.e., in a GRGB arrangement) in odd-numbered rows, and blue, green, red and green OLEDs may be sequentially and repeatedly arranged (i.e., in a BGRG arrangement) in even-numbered rows. However, the arrangements of the OLEDs are not limited to the GRGB and BGRG arrangements.

[0058] Further, in the display panel **110**, each sub-pixel circuit (e.g., SPC**1**) in a first column (e.g., an odd-numbered column) may drive the OLED (e.g., G**1**) in a sub-pixel region (e.g., SPR**1**) the same as a sub-pixel region (e.g., SPR**1**) in which the sub-pixel circuit (e.g., SPC**1**) is disposed, and each sub-pixel circuit (e.g., SPC**2**) in an even-numbered column (e.g., a second column) may drive the OLED (e.g., G**2**) in a sub-pixel region (e.g., SPR**4**) in a row different from a row in which the sub-pixel circuit (e.g., SPC**2**) is disposed. For example, as illustrated in FIG. **1**, a first sub-pixel circuit SPC**1** in a first sub-pixel region SPR**1** may drive the first OLED G**1** in the first sub-pixel region SPR**1**, a second sub-pixel circuit SPC**2** in a second sub-pixel region SPR**2** adjacent to the first sub-pixel region SPR**1** in a row direction (e.g., a direction of a scan line SL**1** and SL**2** or a direction of an emission control line EL**1** and EL**2**) may drive the fourth OLED G**2** in a fourth sub-pixel region SPR**4** adjacent to the second sub-pixel region SPR**2** in the column direction, a third sub-pixel circuit SPC**3** in a third sub-pixel region SPR**3** adjacent to the first sub-pixel region SPR**1** in the column direction may drive the third OLED B**1** in the third sub-pixel region SPR**3**, and a fourth sub-pixel circuit SPC**4** in the fourth sub-pixel region SPR**4** adjacent to the third sub-pixel region SPR**3** in the row direction may drive the second OLED R**1** in the second sub-pixel region SPR**2** adjacent to the fourth sub-pixel region SPR**4** in the column direction.

[0059] Accordingly, the sub-pixel circuits SPC**1** and SPC**2** in a first row (e.g., an odd-numbered row), or the sub-pixel circuits SPC**1** and SPC**2** connected to a first scan line (e.g., an odd-numbered scan line) SL**1** and/or a first emission control line (e.g., an odd-numbered emission control line) EL**1** may drive only the OLEDs G**1** and G**2** emitting the light of the first color (e.g., the green color), and the sub-pixel circuits SPC**3** and SPC**4** in a second row (e.g., an even-numbered row), or the sub-pixel circuits SPC**3** and SPC**4** connected to a second scan line (e.g., an even-numbered scan line) SL**2** and/or a second emission control line (e.g., an even-numbered emission control line) EL**2** may drive only the OLEDs R**1** and B**1** emitting the light of the second color (e.g., the red color) or the third color (e.g., the blue color). Thus, since the sub-pixel circuits SPC**1** and SPC**2** driving the OLEDs G**1** and G**2** emitting the light of the first color (e.g., the green color) are connected to the scan and emission control lines SL**1** and EL**1** separate from the scan and emission control lines SL**2** and EL**2** to which the sub-pixel circuits SPC**3** and SPC**4** driving the OLEDs R**1** and B**1** emitting the light of the second color (e.g., the red color) or the third color (e.g., the blue color), the OLEDs G**1** and G**2** emitting the light of the first color may be driven under a driving condition (e.g., a scan on time, an off period ratio (which may be referred to as an AMOLED off ratio (AOR)), etc.) different from a driving condition for the OLEDs R**1** and B**1** emitting the light of the second color or the third color.

[0060] In some exemplary embodiments, the scan driver **150** may apply a first scan signal SS**1** having a first scan on time (SOT) to the first scan line (e.g., the odd-numbered scan line) SL**1** connected to the sub-pixel circuits SPC**1** and SPC**2** driving the OLEDs G**1** and G**2** emitting the light of the first color, and may apply a second scan signal SS**2** having a second SOT different (in length) from the first SOT to the second scan line (e.g., the even-numbered scan line) SL**2** connected to the sub-pixel circuits SPC**3** and SPC**4** driving the OLEDs R**1** and B**1** emitting the light of the second color or the third color. For example, the first SOT of the first scan signal SS**1** applied to the sub-pixel circuits SPC**1** and SPC**2** driving the OLEDs G**1** and G**2** emitting the light of the first color may be longer than the second SOT of the second scan signal SS**2** applied to the sub-pixel circuits SPC**3** and SPC**4** driving the OLEDs R**1** and B**1** emitting the light of the second color or the third color. In some exemplary embodiments, during the SOT, each sub-pixel circuit SPC**1**, SPC**2**, SPC**3** and SPC**4** may not only store the data signal, but also compensate a threshold voltage of a driving transistor, and thus the SOT of the scan signal SS**1** and SS**2** applied to each sub-pixel circuit SPC**1**, SPC**2**, SPC**3** and SPC**4** may be substantially the same as a threshold voltage compensation time for the driving transistor include in each sub-pixel circuit SPC**1**, SPC**2**, SPC**3** and SPC**4**. Accordingly, a first threshold voltage compensation time for driving transistors included in the sub-pixel circuits SPC**1** and SPC**2** driving the OLEDs G**1** and G**2** emitting the light of the first color may be longer than a second threshold voltage compensation time for driving transistors included in the sub-pixel circuits SPC**3** and SPC**4** driving the OLEDs R**1** and B**1** emitting the light of the second color or the third color.

[0061] Generally, compared with the driving transistor of the sub-pixel circuit SPC**3** and SPC**4** driving the red or green OLED R**1** and B**1**, the driving transistor of the sub-pixel circuit SPC**1** and SPC**2** driving the green OLED G**1** and G**2** may have a relatively high compensation point, and thus may require a relatively long threshold voltage compensation time. As described above, in the OLED display device **100** according to exemplary embodiments, the first threshold voltage compensation time for the driving transistor included in the sub-pixel circuit SPC**1** and SPC**2** driving the green OLED G**1** and G**2** may be longer than the second threshold voltage compensation time for the driving transistor included in the sub-pixel circuit SPC**3** and SPC**4** driving the red or blue OLED R**1** and B**1**, and thus the sub-pixel circuit SPC**1** and SPC**2** driving the green OLED G**1** and G**2** that is vulnerable to a mura may perform a threshold voltage compensation operation for a sufficient

threshold voltage compensation time. Accordingly, the mura of the OLED display device **100** may be reduced or prevented.

[0062] Further, in some exemplary embodiments, the emission driver **170** may apply a first emission control signal SE**1** with a first off period ratio to the first emission control line (e.g., the odd-numbered emission control line) EL**1** connected to the sub-pixel circuits SPC**1** and SPC**2** driving the OLEDs G**1** and G**2** emitting the light of the first color, and may apply a second emission control signal SE**2** with a second off period ratio different from the first off period ratio to the second emission control line (e.g., the even-numbered emission control line) EL**2** connected to the sub-pixel circuits SPC**3** and SPC**4** driving the OLEDs R**1** and B**1** emitting the light of the second color or the third color. For example, the first off period ratio of the first emission control signal SE**1** applied to the sub-pixel circuits SPC**1** and SPC**2** driving the OLEDs G**1** and G**2** emitting the light of the first color may be greater than the second off period ratio of the second emission control signal SE**2** applied to the sub-pixel circuits SPC**3** and SPC**4** driving the OLEDs R**1** and B**1** emitting the light of the second color or the third color. The sub-pixel circuits receiving the first emission control signal SE**1** may drive the OLEDs G**1** and G**2** to emit the light of the first color with the first off period ratio that is increased compared to the second off period ratio for the OLEDs R**1** and B**1** emitting the light of the second color or the third color. Further, the sub-pixel circuits receiving the first emission control signal SE**1** may provide the OLEDs G**1** and G**2** emitting the light of the first color with a driving current that is increased corresponding to the increased first off period ratio. Accordingly, the OLED display device **100** according to exemplary embodiments may allow the driving transistors of the sub-pixel circuits SPC**1** and SPC**2** to generate the increased driving current, or a higher driving circuit, thereby reducing an afterimage caused by a hysteresis of the driving transistors.

[0063] As described above, in the OLED display device **100** according to exemplary embodiments, the OLEDs G**1**, R**1**, B**1** and G**2** may be arranged in a pentile structure such that, in each pixel region PR**1** and PR**2**, one OLED G**1** and G**2** of the first color (e.g., the green color) is disposed and one of the OLED R**1** of the second color (e.g., the red color) or the OLED B**1** of the third color (e.g., the blue color) is alternately disposed. Further, in one column (e.g., the even-numbered column) per two columns, the OLED R**1** in the odd-numbered row may be driven by the sub-pixel circuit SPC**4** in the even-numbered row, and the OLED G**2** in the even-numbered row may be driven by the sub-pixel circuit SPC**2** in the odd-numbered row. Accordingly, the OLED G**1** and G**2** of the first color (e.g., the green color) can be driven under a driving condition (e.g., a scan on time, an AOR, etc.) different from the driving condition for the OLEDs R**1** and B**1** of the second and third colors, and thus the mura and/or the afterimage may be reduced.

[0064] FIG. **2** is a circuit diagram illustrating the display panel of FIG. **1**, and FIG. **3** is a diagram illustrating an exemplary layout of OLEDs included in the display panel of FIG. **1**.

[0065] Referring to FIG. **2**, a display panel **110** may include a plurality of sub-pixel regions SPR**1**, SPR**2**, SPR**3**, SPR**4**, SPR**5**, SPR**6**, SPR**7** and SPR**8**, and, in each sub-pixel region SPR**1**, SPR**2**, SPR**3**, SPR**4**, SPR**5**, SPR**6**, SPR**7** and SPR**8**, one of the OLEDs G**1**, R**1**, B**1**, G**2**, G**3**, B**2**, R**2** and G**4** and one sub-pixel circuit may be disposed. In some exemplary embodiments, green, red, green and blue OLEDs G**1**, R**1**, G**3** and B**2** may be sequentially and repeatedly arranged in an odd-numbered row, and blue, green, red and green OLEDs B**1**, G**2**, R**2** and G**4** may be sequentially and repeatedly arranged in an even-numbered row. However, the arrangements of the OLEDs are not limited to an example of FIG. **2**.

[0066] In some exemplary embodiments, as illustrated in FIG. **2**, each sub-pixel circuit may have a 7T1C structure including seven transistors T**1**, T**2**, T**3**, T**4**, T**5**, T**6** and T**7** and one capacitor CST. For example, each sub-pixel circuit may include a first transistor T**1** which transfers a data signal to one terminal of a second transistor T**2** in response to a scan signal SS**1** and SS**2**, a storage capacitor CST which stores the data signal transferred through the diode-connected second transistor T**2**, the second transistor T**2** which generates a driving current based on the data signal stored in the storage capacitor CST, a third transistor T**3** which diode-connects the second transistor T**2** in response to the scan signal SS**1** and SS**2**, a fourth transistor T**4** which applies an initialization voltage to the storage capacitor CST and a gate of the second transistor T**2** in response to an initialization signal, a fifth transistor T**5** which applies the initialization voltage to the OLED G**1**, R**1**, B**1**, G**2**, G**3**, B**2**, R**2** and G**4** in response to the scan signal SS**1** and SS**2**, a sixth transistor T**6** which connects a line of a high power supply voltage to the second transistor T**2** in response to an emission control signal SE**1** and SE**2**, and a seventh transistor T**7** which connects the second transistor T**2** to the OLED G**1**, R**1**, B**1**, G**2**, G**3**, B**2**, R**2** and G**4** in response to the emission control signal SE**1** and SE**2**. However, the configuration of the sub-pixel circuit is not limited to the example of FIG. **2**.

[0067] Each sub-pixel circuit in an odd-numbered column may drive the OLED G**1**, B**1**, G**3** and R**2** in a sub-pixel region SPR**1**, SPR**3**, SPR**5** and SPR**7** the same as a sub-pixel region SPR**1**, SPR**3**, SPR**5** and SPR**7** in which the sub-pixel circuit is disposed, and each sub-pixel circuit in an even-numbered column may drive the OLED G**2**, R**1**, G**4** and B**2** in a row different from a row in which the sub-pixel circuit is disposed. In the example of FIG. **2**, a second OLED R**1** in a second sub-pixel region SPR**2** in a second column may be connected to a fourth sub-pixel circuit in a fourth sub-pixel region SPR**4**, a fourth OLED G**2** in the fourth sub-pixel region SPR**4** in the second column may be connected to a second sub-pixel circuit in the second sub-pixel region SPR**2**, a sixth OLED B**2** in a sixth sub-pixel region SPR**6** in a fourth column may be connected to an eighth sub-pixel circuit in an eighth sub-pixel region SPR**8**, and an eighth OLED G**4** in the eighth sub-pixel region SPR**8** in the fourth column may be connected to a sixth sub-pixel circuit in the sixth sub-pixel region SPR**6**.

[0068] In some exemplary embodiments, as illustrated in FIG. **3**, each OLED G**1**, B**1**, G**3** and R**2** in the odd-numbered column may include an anode **111**, **115**, **121** and **125** formed to be connected to (a drain of the seventh transistor T**7** of) a sub-pixel circuit in a sub-pixel region SPR**1**, SPR**3**, SPR**5** and SPR**7** the same as a sub-pixel region SPR**1**, SPR**3**, SPR**5** and SPR**7** in which the OLED G**1**, B**1**, G**3** and R**2** is disposed, and an organic light emitting layer **112**, **116**, **122** and **126** formed on the anode **111**, **115**, **121** and **125**. However, each OLED G**2**, R**1**, G**4** and B**2** in the even-numbered column may include not only an anode **113**, **117**,

123 and **127** and an organic light emitting layer **114**, **118**, **124** and **128**, but also an anode extension portion **113-1**, **117-1**, **123-1** and **127-1** formed to be connected to (a drain of the seventh transistor T**7** of) a sub-pixel circuit in a row different from a row in which the OLED G**2**, R**1**, G**4** and B**2** is disposed. In some exemplary embodiments, the anode **113**, **117**, **123** and **127** and the anode extension portion **113-1**, **117-1**, **123-1** and **127-1** may be formed integrally or in a unitary structure by the same process. Thus, an additional process dedicated for the anode extension portion **113-1**, **117-1**, **123-1** and **127-1** may not be required.

[0069] Further, as illustrated in FIG. **2**, sub-pixel circuits driving green OLEDs G**1**, G**2**, G**3** and G**4** may receive the same first scan signal SS**1** and the same first emission control signal SE**1**, and sub-pixel circuits driving red and blue OLEDs B**1**, R**1**, R**2** and B**2** may receive a second scan signal SS**2** different from the first scan signal SS**1** and a second emission control signal SE**2** different from the first emission control signal SE**1**. Since the sub-pixel circuits driving the green OLEDs G**1**, G**2**, G**3** and G**4** receive the first scan signal SS**1** and the first emission control signal SE**1** different from the second scan signal SS**2** and the second emission control signal SE**2** applied to the sub-pixel circuits driving the red and blue OLEDs B**1**, R**1**, R**2** and B**2**, the green OLEDs G**1**, G**2**, G**3** and G**4** and the red and blue OLEDs B**1**, R**1**, R**2** and B**2** may be driven under different driving conditions (e.g., different SOTs, different off period ratios, etc.).

[0070] FIG. **4** is a timing diagram illustrating scan signals of a conventional OLED display device and scan signals of an OLED display device according to the principles and exemplary embodiments of the invention.

[0071] In FIG. **4**, **210** represents conventional scan signals CSS**1**, CSS**2**, CSS**3** and CSS**4** and a conventional data signal CSD, and **230** represents scan signals SS**1**, SS**2**, SS**3** and SS**4** and a data signal SD of an OLED display device according to exemplary embodiments of the invention.

[0072] The conventional scan signals CSS**1**, CSS**2**, CSS**3** and CSS**4** have the same scan on time CSOT. However, in the OLED display device according to exemplary embodiments, a second scan on time SOT**2** of scan signals SS**2** and SS**4** applied to sub-pixel circuits in even-numbered rows for driving red and blue OLEDs may be decreased compared with the conventional scan on time CSOT, and a first scan on time SOT**1** of scan signals SS**1** and SS**3** applied to sub-pixel circuits in odd-numbered rows for driving green OLEDs may be increased compared with the conventional scan on time CSOT. Further, referring to FIG. **2**, during the scan on time SOT**1** and SOT**2**, a first transistor T**1** may be turned on to transfer the data signal SD, a third transistor T**3** may be turned on to diode-connect a second transistor T**2**, and thus a threshold voltage compensation operation that a threshold voltage of the second transistor T**2** is subtracted from the data signal SD in a storage capacitor CST may be performed. Accordingly, since the first scan on time SOT**1** of the scan signals SS**1** and SS**3** applied to the sub-pixel circuits driving the green OLEDs is increased, a threshold voltage compensation time for the driving transistors T**2** included in the sub-pixel circuits driving the green OLEDs may be increased, and thus a mura of the OLED display device may be reduced or prevented.

[0073] FIG. **5** is a block diagram illustrating a scan driver included in an OLED display device constructed according to an exemplary embodiment of the invention, FIG. **6** is a circuit diagram illustrating an example of each stage included in the scan driver of FIG. **5**, and FIG. **7** is a timing diagram for describing an example of an operation of the scan driver of FIG. **5**.

[0074] Referring to FIG. **5**, a scan driver **150** included in an OLED display device according to exemplary embodiments may include a plurality of stages **152**, **154**, **156** and **158** which output a plurality of scan signals SS**1**, SS**2**, SS**3** and SS**4** in response to a start signal FLM (or a previous scan signal), a first clock signal CLK**1** and a second clock signal CLK**2**.

[0075] In some exemplary embodiments, as illustrated in FIG. **6**, each stage **152**a may include a first transistor M**1** which transfers the start signal FLM or the previous scan signal PSS to a first node N**1** in response to the first clock signal CLK**1** (or the second clock signal CLK**2** in case of an even-numbered stage **154** and **158**), a second transistor M**2** which transfers a high gate voltage VGH to a fourth node N**4** in response to a voltage of a third node N**3**, a third transistor M**3** which transfers a voltage of the fourth node N**4** to the first node N**1** in response to the second clock signal CLK**2** (or the first clock signal CLK**1** in case of an even-numbered stage **154** and **158**), a fourth transistor M**4** which transfers the first clock signal CLK**1** (or the second clock signal CLK**2** in case of an even-numbered stage **154** and **158**) to the third node N**3** in response to a voltage of the first node N**1**, a fifth transistor M**5** which transfers a low gate voltage VGL to the third node N**3** in response to the first clock signal CLK**1** (or the second clock signal CLK**2** in case of an even-numbered stage **154** and **158**), a sixth transistor M**6** which outputs the high gate voltage VGH as the scan signal SS**1** to a scan output node NS in response to the voltage of the third node N**3**, a seventh transistor M**7** which outputs the second clock signal CLK**2** (or the first clock signal CLK**1** in case of an even-numbered stage **154** and **158**) as the scan signal SS**1** to the scan output node NS in response to a voltage of a second node N**2**, an eighth transistor M**8** which transfers the voltage of the first node N**1** to the second node N**2** in response to the low gate voltage VGL, a first capacitor C**1** connected between a line of the high gate voltage VGH and the third node N**3**, and a second capacitor C**2** connected between the second node N**2** and the scan output node NS. However, the configuration of each stage **152**, **154**, **156** and **158** of the scan driver **150** according to exemplary embodiments is not limited to the example of FIG. **6**.

[0076] Referring to FIGS. **5** and **7**, the second clock signal CLK**2** may have an on period longer than an on period of the first clock signal CLK**1**. Thus, odd-numbered stages **152** and **156** may output the scan signals SS**1** and SS**3** having a relatively long scan on time SOT**1** during the relatively long on period of the second clock signal CLK**2**, and even-numbered stages **154** and **158** may output the scan signals SS**2** and SS**4** having a relatively short scan on time SOT**2** during the relatively short on period of the first clock signal CLK**1**. Accordingly, sub-pixel circuits in odd-numbered rows for driving green OLEDs may receive the scan signals SS**1** and SS**3** having the relatively long scan on time SOT**1**, a sufficient threshold voltage compensation time for driving transistors included in the sub-pixel circuits driving the green OLEDs may be obtained, and thus a mura of an OLED display device may be reduced or prevented.

[0077] FIG. **8** is a timing diagram illustrating emission control signals of a conventional OLED display device and emission control signals of an OLED display device con-

structed according to the principles and exemplary embodiments of the invention, and FIG. **9** is a graph illustrating the increase of a driving current level according to the increase of an AMOLED off ratio (AOR) in an OLED display device constructed according to the principles and exemplary embodiments of the invention.

[0078] In FIG. **8**, **310** represents conventional emission control signals CSE**1**, CSE**2**, CSE**3** and CSE**4**, and **330** represents emission control signals SE**1**, SE**2**, SE**3** and SE**4** of an OLED display device according to exemplary embodiments. Each frame period FP may include a non-emission period NEP and an emission period EP. For example, the non-emission period NEP may be a period in which the emission control signals CSE**1**, CSE**2**, CSE**3**, CSE**4**, SE**1**, SE**2**, SE**3** and SE**4** have an off level (e.g., a high level), and may include a scan period and/or an initialization period. The emission period EP may be a period in which sixth and seventh transistors T**6** and T**7** are turned on to allow OLEDs to emit light in response to the emission control signals CSE**1**, CSE**2**, CSE**3**, CSE**4**, SE**1**, SE**2**, SE**3** and SE**4** having an on level (e.g., a low level).

[0079] During the emission period EP, the conventional emission control signals CSE**1**, CSE**2**, CSE**3** and CSE**4** may be maintained as the on level. However, in the OLED display device according to exemplary embodiments, at least a portion SE**1** and SE**3** of the emission control signals SE**1**, SE**2**, SE**3** and SE**4** may have on periods ONP and off periods OFFP within the emission period EP. In some exemplary embodiments, a first off period ratio (e.g., a ratio of a sum of lengths of the off periods OFFP to a length of the emission period EP) of the emission control signals SE**1** and SE**3** applied to sub-pixel circuits in odd-numbered rows for driving green OLEDs may be greater than a second off period ratio of the emission control signals SE**2** and SE**4** applied to sub-pixel circuits in even-numbered rows for driving red and blue OLEDs. For example, as illustrated in FIG. **8**, the emission control signals SE**2** and SE**4** applied to the sub-pixel circuits in the even-numbered rows may be maintained as the on level, or may have an off period ratio of about 0%, and the emission control signals SE**1** and SE**3** applied to the sub-pixel circuits in the odd-numbered rows may have the off periods OFFP corresponding to a half of the emission period EP, or may have an off period ratio of about 50%. Thus, the sub-pixel circuits receiving the emission control signals SE**2** and SE**4** having the off period ratio of about 0% may drive the red and blue OLEDs with the off period ratio of about 0%, but the sub-pixel circuits receiving the emission control signals SE**1** and SE**3** having the off period ratio of about 50% may drive the green OLEDs with the off period ratio of about 50%. That is, the green OLEDs may be driven with an increased off period ratio.

[0080] Further, the sub-pixel circuits in the odd-numbered rows may provide the green OLEDs with a driving current that is increased corresponding to the increased off period ratio. For example, as illustrated in FIG. **9**, if a second off period ratio AOR**2** is increased to about 50% compared with a first off period ratio AOR**1** of about 0%, the driving current provided to the green OLEDs may be increased from a first driving current level CL**1** to a second driving current level CL**2** such that an area **430** defined by the second off period ratio AOR**2** and the second driving current level CL**2** becomes substantially the same as an area **410** defined by the first off period ratio AOR**1** and the first driving current level CL**1**. Accordingly, driving transistors included in the sub-pixels driving the green OLEDs may generate the increased driving current, or a higher driving current, thereby reducing an afterimage caused by a hysteresis of the driving transistors.

[0081] FIG. **10** is a block diagram illustrating an OLED display device constructed according to the principles and another exemplary embodiment of the invention.

[0082] An OLED display device **500** of FIG. **10** may have a similar configuration and a similar operation to those of an OLED display device **100** of FIG. **1**, except for the configuration of a display panel **510**.

[0083] The display panel **510** may have a plurality of pixel regions PR**1** and PR**2**, and each pixel region PR**1** and PR**2** may include two sub-pixel regions SPR**1**, SPR**2**, SPR**3** and SPR**4**. Further, in each sub-pixel region SPR**1**, SPR**2**, SPR**3** and SPR**4**, one OLED G**1**, R**1**, B**1** and G**2** and one sub-pixel circuit SPC**1**, SPC**2**, SPC**3** and SPC**4** may be disposed. In the display panel **510** of FIG. **10**, unlike a display panel **110** of FIG. **1**, each sub-pixel circuit SPC**1**, SPC**2**, SPC**3** and SPC**4** may drive the OLED G**1**, R**1**, B**1** and G**2** in a sub-pixel region SPR**1**, SPR**2**, SPR**3** and SPR**4** the same as a sub-pixel region SPR**1**, SPR**2**, SPR**3** and SPR**4** in which the sub-pixel circuit SPC**1**, SPC**2**, SPC**3** and SPC**4** is disposed.

[0084] However, a sub-pixel circuit (e.g., SPC**2**) in an even-numbered column may be connected to a scan line (e.g., SL**2**) and/or an emission control line (e.g., EL**2**) of a row different from a row in which the sub-pixel circuit (e.g., SPC**2**) is disposed. For example, a fourth sub-pixel circuit SPC**4** in a fourth sub-pixel region SPR**4** may be connected by a first auxiliary scan line ASL**1** to a first scan line SL**1** extending in a row direction through a first sub-pixel region SPR**1** and a second sub-pixel region SPR**2**, and may be connected by a first auxiliary emission control line AEL**1** to a first emission control line EL**1** extending in the row direction through the first sub-pixel region SPR**1** and the second sub-pixel region SPR**2**. Further, a second sub-pixel circuit SPC**2** in the second sub-pixel region SPR**2** may be connected by a second auxiliary scan line ASL**2** to a second scan line SL**2** extending in the row direction through a third sub-pixel region SPR**3** and the fourth sub-pixel region SPR**4**, and may be connected by a second auxiliary emission control line ASL**2** to a second emission control line EL**2** extending in the row direction through the third sub-pixel region SPR**3** and the fourth sub-pixel region SPR**4**. Accordingly, first and fourth sub-pixel circuits SPC**1** and SPC**4** driving green OLEDs G**1** and G**2** may be connected to the scan and emission control lines SL**1** and EL**1** separate from the scan and emission control lines SL**2** and EL**2** connected to second and third sub-pixels SPC**2** and SPC**3** driving red and blue OLEDs R**1** and B**1**, and thus the green OLEDs G**1** and G**2** and the red and blue OLEDs R**1** and B**1** may be driven under different driving conditions (e.g., different SOTs, different off period ratios, etc.).

[0085] FIG. **11** is a block diagram illustrating an electronic device including an OLED display device constructed according to the principles and an exemplary embodiment of the invention.

[0086] Referring to FIG. **11**, an electronic device **1100** may include a processor **1110**, a memory device **1120**, a storage device **1130**, an input/output (I/O) device **1140**, a power supply **1150**, and an OLED display device **1160**. The electronic device **1100** may further include a plurality of

ports for communicating a video card, a sound card, a memory card, a universal serial bus (USB) device, other electric devices, etc.

[0087] The processor **1110** may perform various computing functions or tasks. The processor **1110** may be an application processor (AP), a micro processor, a central processing unit (CPU), etc. The processor **1110** may be coupled to other components via an address bus, a control bus, a data bus, etc. Further, in some exemplary embodiments, the processor **1110** may be further coupled to an extended bus such as a peripheral component interconnection (PCI) bus.

[0088] The memory device **1120** may store data for operations of the electronic device **1100**. For example, the memory device **1120** may include at least one non-volatile memory device such as an erasable programmable read-only memory (EPROM) device, an electrically erasable programmable read-only memory (EEPROM) device, a flash memory device, a phase change random access memory (PRAM) device, a resistance random access memory (RRAM) device, a nano floating gate memory (NFGM) device, a polymer random access memory (PoRAM) device, a magnetic random access memory (MRAM) device, a ferroelectric random access memory (FRAM) device, etc, and/or at least one volatile memory device such as a dynamic random access memory (DRAM) device, a static random access memory (SRAM) device, a mobile dynamic random access memory (mobile DRAM) device, etc.

[0089] The storage device **1130** may be a solid state drive (SSD) device, a hard disk drive (HDD) device, a CD-ROM device, etc. The I/O device **1140** may be an input device such as a keyboard, a keypad, a mouse, a touch screen, etc, and an output device such as a printer, a speaker, etc. The power supply **1150** may supply power for operations of the electronic device **1100**.

[0090] In the OLED display device **1160**, OLEDs may be arranged in a pentile structure such that, in each pixel region, an OLED of a first color (e.g., a green color) is disposed and one of an OLED of a second color (e.g., a red color) or an OLED of a third color (e.g., a blue color) alternately disposed. Further, in one column (e.g., an even-numbered column) per two columns, an OLED in an odd-numbered row may be driven by a sub-pixel circuit in an even-numbered row, and an OLED in the even-numbered row may be driven by a sub-pixel circuit in the odd-numbered row. Accordingly, the OLED of the first color (e.g., the green color) can be driven under a driving condition (e.g., a scan on time, an AOR, etc.) different from a driving condition for the OLEDs of the second and third colors, and thus a mura and/or an afterimage may be reduced.

[0091] According to exemplary embodiments, the electronic device **1100** may be any electronic device including the OLED display device **1160**, such as a cellular phone, a smart phone, a tablet computer, a wearable device, a personal digital assistant (PDA), a portable multimedia player (PMP), a digital camera, a music player, a portable game console, a navigation system, a digital television, a 3D television, a personal computer (PC), a home appliance, a laptop computer, etc.

[0092] Although certain exemplary embodiments and implementations have been described herein, other embodiments and modifications will be apparent from this description. Accordingly, the inventive concepts are not limited to such embodiments, but rather to the broader scope of the appended claims and various obvious modifications and equivalent arrangements as would be apparent to a person of ordinary skill in the art.

What is claimed is:

1. A display panel of an organic light emitting diode (OLED) display device, the display panel comprising:

a first OLED disposed in a first sub-pixel region, and configured to emit light of a first color;

a second OLED disposed in a second sub-pixel region adjacent to the first sub-pixel region in a row direction, and configured to emit light of a second color;

a third OLED disposed in a third sub-pixel region adjacent to the first sub-pixel region in a column direction, and configured to emit light of a third color;

a fourth OLED disposed in a fourth sub-pixel region adjacent to the second sub-pixel region in the column direction and adjacent to the third sub-pixel region in the row direction, and configured to emit light of the first color;

a first sub-pixel circuit disposed in the first sub-pixel region, and configured to drive the first OLED in the first sub-pixel region;

a second sub-pixel circuit disposed in the second sub-pixel region, and configured to is drive the fourth OLED in the fourth sub-pixel region;

a third sub-pixel circuit disposed in the third sub-pixel region, and configured to drive the third OLED in the third sub-pixel region; and

a fourth sub-pixel circuit disposed in the fourth sub-pixel region, and configured to drive the second OLED in the second sub-pixel region.

2. The display panel of claim **1**, wherein the first and fourth OLEDs are green OLEDs configured to emit green light, the second OLED is a red OLED configured to emit red light, and the third OLED is a blue OLED configured to emit blue light.

3. The display panel of claim **1**, wherein the second OLED in the second sub-pixel region includes an anode extension portion connected to the fourth sub-pixel circuit, and

wherein the fourth OLED in the fourth sub-pixel region includes another anode extension portion connected to the second sub-pixel circuit.

4. The display panel of claim **1**, wherein the first and second sub-pixel circuits each receives a first scan signal having substantially the same value through a first scan line, and

wherein the third and fourth sub-pixel circuits each receives a second scan signal having substantially the same value through a second scan line.

5. The display panel of claim **4**, wherein a first scan on time (SOT) of the first scan signal applied to the first and second sub-pixel circuits is different from a second SOT of the second scan signal applied to the third and fourth sub-pixel circuits.

6. The display panel of claim **4**, wherein a first SOT of the first scan signal applied to the first and second sub-pixel circuits is longer than a second SOT of the second scan signal applied to the third and fourth sub-pixel circuits.

7. The display panel of claim **6**, wherein the first and second sub-pixel circuits further comprise first driving transistors, the third and fourth sub-pixel circuits further comprise second driving transistors a first threshold voltage

compensation time for the first driving transistors is longer than a second threshold voltage compensation time for the second driving transistors.

8. The display panel of claim **1**, wherein the first and second sub-pixel circuits receive a first emission control signal having substantially the same value through a first emission control line, and

wherein the third and fourth sub-pixel circuits receive a second emission control signal having substantially the same value through a second emission control line.

9. The display panel of claim **8**, wherein a first off period ratio of the first emission control signal applied to the first and second sub-pixel circuits is different from a second off period ratio of the second emission control applied to the third and fourth sub-pixel circuits.

10. The display panel of claim **8**, wherein a first off period ratio of the first emission control signal applied to the first and second sub-pixel circuits is greater than a second off period ratio of the second emission control applied to the third and fourth sub-pixel circuits.

11. The display panel of claim **10**, wherein the first and second sub-pixel circuits drive the first and fourth OLEDs to emit the light of the first color with the first off period ratio that is increased compared to the second off period ratio for the second and third OLEDs.

12. The display panel of claim **11**, wherein the first and second sub-pixel circuits provide the first and fourth OLEDs with a driving current corresponding to the increased first off period ratio, the driving current being provided to the first and fourth OLEDs being greater than driving current provided to the second and third OLEDs.

13. A display panel of an organic light emitting diode (OLED) display device, comprising:

a first OLED disposed in a first sub-pixel region, and configured to emit light of a first color;

a second OLED disposed in a second sub-pixel region adjacent to the first sub-pixel region in a row direction, and configured to emit light of a second color;

a third OLED disposed in a third sub-pixel region adjacent to the first sub-pixel region in a column direction, and configured to emit light of a third color;

a fourth OLED disposed in a fourth sub-pixel region adjacent to the second sub-pixel region in the column direction and adjacent to the third sub-pixel region in the row direction, and configured to emit light of the first color;

a first sub-pixel circuit configured to drive the first OLED;

a second sub-pixel circuit configured to drive the second OLED;

a third sub-pixel circuit configured to drive the third OLED;

a fourth sub-pixel circuit configured to drive the fourth OLED;

a first scan line extending in the row direction through the first sub-pixel region and the second sub-pixel region, and connected to the first sub-pixel circuit;

a second scan line extending in the row direction through the third sub-pixel region and the fourth sub-pixel region, and connected to the third sub-pixel circuit;

a first auxiliary scan line connecting the first scan line to the fourth sub-pixel circuit; and

a second auxiliary scan line connecting the second scan line to the third sub-pixel circuit.

14. The display panel of claim **13**, wherein the first sub-pixel circuit receives a first scan signal through the first scan line,

wherein the fourth sub-pixel circuit is configured to receive the first scan signal through the first scan line and the first auxiliary scan line,

wherein the third sub-pixel circuit is configured to receive a second scan signal through the second scan line, and

wherein the second sub-pixel circuit is configured to receive the second scan signal through the second scan line and the second auxiliary scan line.

15. The display panel of claim **14**, wherein a first scan on time (SOT) of the first scan signal applied to the first and fourth sub-pixel circuits is longer than a second SOT of the second scan signal applied to the second and third sub-pixel circuits.

16. The display panel of claim **13**, further comprising:

a first emission control line extending in the row direction through the first sub-pixel region and the second sub-pixel region, and connected to the first sub-pixel circuit;

a second emission control line extending in the row direction through the third sub-pixel region and the fourth sub-pixel region, and connected to the third sub-pixel circuit;

a first auxiliary emission control line connecting the first emission control line to the fourth sub-pixel circuit; and

a second auxiliary emission control line connecting the second emission control line to the third sub-pixel circuit.

17. The display panel of claim **16**, wherein the first sub-pixel circuit is configured to receive a first emission control signal through the first emission control line,

wherein the fourth sub-pixel circuit is configured to receive the first emission control signal through the first emission control line and the first auxiliary emission control line,

wherein the third sub-pixel circuit in the third sub-pixel region is configured to receive a second emission control signal through the second emission control line, and

wherein the second sub-pixel circuit is configured to receive the second emission control signal through the second emission control line and the second auxiliary emission control line.

18. The display panel of claim **17**, wherein a first off period ratio of the first emission control signal applied to the first and fourth sub-pixel circuits is greater than a second off period ratio of the second emission control applied to the second and third sub-pixel circuits.

19. The display panel of claim **18**, wherein the first and fourth sub-pixel circuits are configured to drive the first and fourth OLEDs to emit the light of the first color with the first off period ratio that is increased compared to the second off period ratio for the second and third OLEDs.

20. An organic light emitting diode (OLED) display device, comprising:

a display panel;

a data driver configured to provide data signals to the display panel;

a scan driver configured to provide scan signals to the display panel;

an emission driver configured to provide emission control signals to the display panel; and

a timing controller configured to control the data driver, the scan driver and the emission driver,

wherein the display panel comprises:

a first OLED disposed in a first sub-pixel region, and configured to emit light of a first color;

a second OLED disposed in a second sub-pixel region adjacent to the first sub-pixel region in a row direction, and configured to emit light of a second color;

a third OLED disposed in a third sub-pixel region adjacent to the first sub-pixel region in a column direction, and configured to emit light of a third color;

a fourth OLED disposed in a fourth sub-pixel region adjacent to the second sub-pixel region in the column direction and adjacent to the third sub-pixel region in the row direction, and configured to emit light of the first color;

a first sub-pixel circuit disposed in the first sub-pixel region, and configured to drive the first OLED in the first sub-pixel region;

a second sub-pixel circuit disposed in the second sub-pixel region, and configured to drive the fourth OLED in the fourth sub-pixel region;

a third sub-pixel circuit disposed in the third sub-pixel region, and configured to drive the third OLED in the third sub-pixel region; and

a fourth sub-pixel circuit disposed in the fourth sub-pixel region, and configured to drive the second OLED in the second sub-pixel region.

* * * * *

专利名称(译)	具有pentile像素结构的有机发光二极管显示装置的显示面板		
公开(公告)号	US20190279563A1	公开(公告)日	2019-09-12
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[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	HWANG YOUNG IN GIL ELLY LEE JINA JO JOOHYEON		
发明人	HWANG, YOUNG-IN GIL, ELLY KIM, EUNGTAEK LEE, JINA JO, JOOHYEON CHU, SEONGBAIK		
IPC分类号	G09G3/3225 H01L27/32 G09G3/3266 G09G3/3275		
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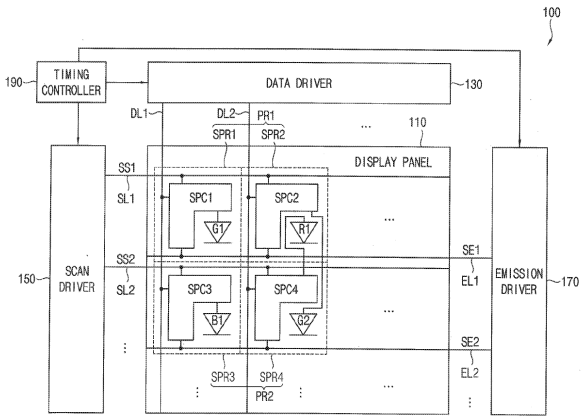
摘要(译)

OLED显示装置的显示面板包括设置在第一子像素区域中的第一OLED，设置在沿行方向与第一子像素区域相邻的第二子像素区域中的第二OLED，设置在第一OLED中的第三OLED在列方向上与第一子像素区域相邻的第三子像素区域，在列方向上与第二子像素区域相邻且与第三子像素相邻的第四子像素区域中的第四OLED行方向上的区域，设置在第一子像素区域中的第一子像素电路和设置在第四子像素区域中的第四子像素电路，均配置为驱动第一OLED，第二子像素电路设置在第二子像素区域中，用于驱动第四OLED，第三子像素电路设置在第三子像素区域中，用于驱动第三OLED。